

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising a hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, and tantalum oxide, ~~titanium oxide, zirconium oxide and aluminum oxide.~~

Claim 2 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a perovskite.

Claim 3 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a material with a dielectric constant of 20 or more.

Claim 4 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a ferroelectric material.

Claim 5 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a layered superlattice material.

Claim 6 (Original) An integrated circuit as in claim 5 wherein said layered superlattice material comprises one or more of the following chemical elements: strontium, calcium, barium, bismuth, lead, yttrium, scandium, lanthanum, antimony, chromium, thallium, titanium, tantalum, hafnium, tungsten, niobium, zirconium, oxygen, fluorine and chlorine.

Claim 7 (Original) An integrated circuit as in claim 6 wherein said layered superlattice material comprises a material selected from the group comprising strontium bismuth tantalate, strontium bismuth niobate and solid solutions thereof.

Claim 8 (Original) An integrated circuit as in claim 7 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to the stoichiometric formula $\text{SrBi}_y(\text{Ta}_{1-x}\text{Nb}_x)_2\text{O}_9$, wherein $0 \leq x \leq 1$ and $2.0 \leq y \leq 2.2$.

Claim 9 (Canceled)

Claim 10 (Currently Amended) An integrated circuit as in claim 9 1 wherein

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said hydrogen barrier layer material comprises strontium tantalate.

Claim 11 (Original) An integrated circuit as in claim 1 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

Claim 12 (Original) An integrated circuit as in claim 11 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

Claim 13 (Original) An integrated circuit as in claim 12 wherein said ferroelectric material comprises a layered superlattice material.

 Claim 14 (Original) An integrated circuit as in claim 1 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

Claim 15 (Original) An integrated circuit as in claim 14 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

Claim 16 (Original) An integrated circuit as in claim 15 wherein said ferroelectric material comprises a layered superlattice material.

Claim 17 (Original) An integrated circuit as in claim 1 wherein said hydrogen barrier layer is between 30 nanometers and 100 nanometers (nm) thick.

Claim 18 (Original) An integrated circuit as in claim 17 wherein said hydrogen barrier layer is between 70 nm and 90 nm thick.

Claim 19 (Canceled)

Claim 20 (Original) An integrated circuit as in claim 1 wherein said integrated circuit includes a semiconducting substrate, and said metal oxide material is located between said hydrogen barrier layer and said substrate.

Claim 21 (Original) An integrated circuit as in claim 20 wherein said integrated circuit includes a wiring layer and a second hydrogen barrier layer located above said wiring layer.

Claim 22 (Original) An integrated circuit as in claim 1 wherein said integrated circuit further includes a substrate and a wiring layer, said metal oxide material is located

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between said wiring layer and said substrate, and said hydrogen barrier layer is located above said wiring layer.

Claim 23 (Original) An integrated circuit as in claim 1 wherein said hydrogen barrier layer material comprises a primary hydrogen barrier layer material and said hydrogen barrier layer further includes a supplemental hydrogen barrier layer material different from said primary hydrogen barrier layer material.

Claim 24 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer material comprises silicon nitride or alumina.

Claim 25 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is conducting.

Claim 26 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is insulating.

Claim 27 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is adjacent to and in direct contact with said primary hydrogen barrier layer.

Claim 28 (Currently Amended) An integrated circuit comprising:
a thin film of metal oxide material; and
a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising an amorphous hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, and tantalum oxide.

Claim 29 (Original) An integrated circuit as in claim 28 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

Claim 30 (Original) An integrated circuit as in claim 29 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

Claim 31 (Original) An integrated circuit as in claim 30 wherein said ferroelectric material comprises a layered superlattice material.

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Claim 32 (Original) An integrated circuit as in claim 28 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

Claim 33 (Original) An integrated circuit as in claim 32 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

Claim 34 (Original) An integrated circuit as in claim 33 wherein said ferroelectric material comprises a layered superlattice material.

Claim 35 (Original) An integrated circuit as in claim 28 wherein said hydrogen barrier layer is between 30 nanometers and 100 nanometers (nm) thick.

Claim 36 (Original) An integrated circuit as in claim 28 wherein said amorphous material has a crystallization temperature of greater than 650°C.

Claim 37 (Original) An integrated circuit as in claim 28 wherein said amorphous material comprises a primary hydrogen barrier layer and wherein said integrated circuit further comprises a supplemental hydrogen barrier layer that is crystalline.

Claim 38 (Currently Amended) An integrated circuit comprising:
a thin film of metal oxide material; and

a multiple layer hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising a primary hydrogen barrier layer material and a supplemental hydrogen barrier layer material, said primary hydrogen barrier layer material being different than said supplemental hydrogen barrier layer material, and wherein said primary and supplemental materials are either both conducting or both insulating, and wherein said primary hydrogen barrier layer and said supplemental hydrogen barrier layer both inhibit diffusion of hydrogen to said metal oxide material from essentially the same direction over the majority of the length of the shortest one of said primary hydrogen barrier layer and said supplemental hydrogen barrier layer.

Claim 39 (Original) An integrated circuit as in claim 38 wherein said supplemental material is located in contact with said primary material.

Claim 40 (Original) An integrated circuit as in claim 38 wherein said primary

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material and said secondary material are both conducting.

Claim 41 (Original) An integrated circuit as in claim 38 wherein said primary material and said secondary material are both insulating.

Claim 42 (Original) An integrated circuit as in claim 38 wherein said primary material is more compatible with said metal oxide material and is located closer to said metal oxide material.

Claim 43 (Original) An integrated circuit as in claim 42 wherein said primary material comprises one of the chemical elements that is in said metal oxide material.

 Claim 44 (Original) An integrated circuit as in claim 43 wherein said metal oxide material is a layered superlattice material.

Claim 45 (Original) An integrated circuit as in claim 44 wherein said primary material comprises material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide.

Claim 46 (Original) An integrated circuit as in claim 38 wherein said supplemental material comprises a material selected from the group consisting of silicon nitride and allumina.

Claims 47 – 67 (Withdrawn)

Claim 68 (New) An integrated circuit as in claim 38 wherein said primary hydrogen barrier layer material comprises amorphous material and wherein said supplemental hydrogen barrier layer material comprises crystalline material.
